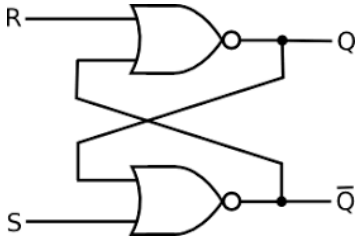
CMPE212 Lab10- Experimenting with S-R Latch and JK Flip-Flop

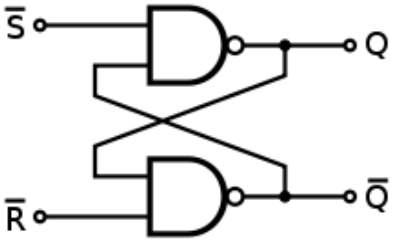
Objective

Implementation of S-R latch with NOR and NAND gates. Experimenting with JK flip-flops.

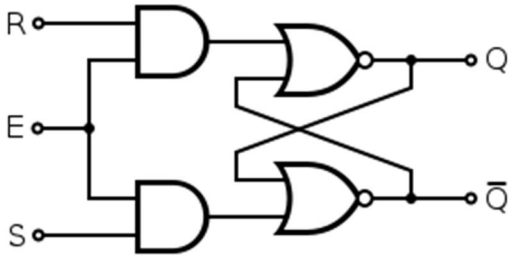
Instructions-

1. Implement the S-R latch with NOR and NAND gates. Vary the inputs and check if the characteristic table holds true.





2. Build a gated S-R latch with NOR gates. Vary the inputs and observe how the enable works.



3. Take your JK flip-flop IC- 74LS76 and build a circuit to observe its functionality. Make the characteristic table and check if it's correct.

4. Show the results to the TAs.

NOTES: 1) Don't vary the inputs randomly like previous labs. Note down the present output first and then vary the inputs. Now note down the outputs in your characteristic table.

2) Give the clock signal very carefully. Try to do it at once. See the consequence of adding a 1000µF capacitor in parallel with the switch.

Remarks

- Connect the DIP switch properly.
- Connect resistors in series to your output LED.
- Don't forget to return the breadboards and multimeters with cables.