CMPE212 Lab5- Verifying De Morgan's Law using Verilog and Logic Gates

Objective

To verify the De Morgan's Law in Verilog. To the De Morgan's Law using hardware.

Verilog

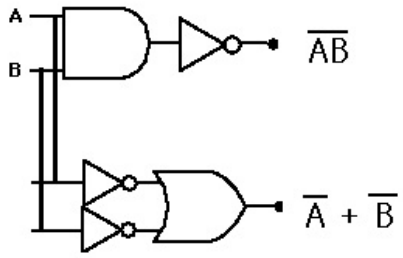
1. Write and execute two different Verilog codes to find the truth tables for the expression $C = \overline{AB}$ and the expression $C = \bar{A} + \bar{B}$. They must be identical.

2. Write and execute two different Verilog codes to find the truth tables for the expression $C = \overline{A + B}$ and the expression $C = \bar{A}.\bar{B}$. They must be identical.

Note: You can use previous module and testbench files as templates.

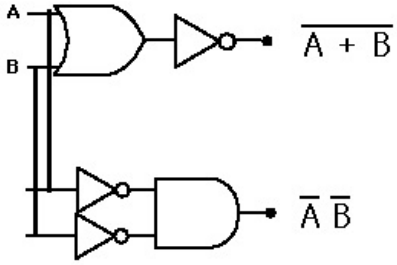
Hardware

1. Collect the instruments and build the following circuit on the breadboard:



2. Vary the inputs and observe the outputs. The two outputs should be identical.

3. Construct the following circuit on the breadboard-



4. Vary the inputs and observe the outputs. The two outputs should be identical.

Notes: i) You can use NAND and NOR gates in the previous circuits.
ii) Refer to the discussion slides for the IC pinouts.