CMPE212 Lab2 Building and Verifying Half-Adder Circuit in Verilog

Objective

To build and verify half-adder circuit in Verilog.

Verilog

1. Connect to the Linux GL server using whichever terminal program you prefer, i.e. putty.exe
   Hostname is "gl.umbc.edu" and connection type "SSH"
   For mac/linux, open terminal and enter "ssh gl.umbc.edu".
2. Open nano editor using the command **nano.**
3. Create your module-
   Write down your Verilog code and save the file as Half_Adder.v

```
module ha(Sum,Carry,A,B);
            Input A,B;
            Output Sum,Carry;

            assign Sum=A^B;
            assign Carry=A&B;
endmodule
```

4. Create your test bench-
   Write down your Verilog code and save the file as Half_Adder_tb.v

```
module ha_tb();
      reg A;
      reg B;
      wire Sum;
      wire Carry;

ha uut(Sum, Carry, A, B);

      initial
      begin
      //Initialize inputs
      $monitor ("input: A =%b, B = %b Output: S = %b, C = %b",A, B, Sum, Carry)$
                                    A=0; B=0;
                        #20  A=0; B=1;
                        #20  A=1; B=0;
                        #20  A=1; B=1;
                        #20;
       end
endmodule
```

5. Finally, run and compile your program using the command:

```
verilog Half_Adder_tb.v Half_Adder.v
```

6. Show your output to the TA.

7. Follow the next instructions from the TA in the lab.

Remarks

If you haven't setup Verilog in the first lab, follow the discussion slides "Running the Verilog for the 1st time". Have fun and ask questions to your TAs.