Seagate demonstrates Ultra SCSI 320

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Just in case SCSI 160 isn't fast enough for you Seagate has upped the proverbial performance bar by demonstrating Ultra SCSI 320 technology in action. The good news is that it's backwards compatible with the slower, outdated, SCSI 160 technology.

Seagate Technology today announced that it has demonstrated Ultra320 SCSI disc drive technology that supports the industry proposals for the SPI-4 (Ultra320 SCSI) standard. The demonstration, conducted with a fully-integrated 320 Mbytes/sec SCSI initiator and target controller designed by Seagate, delivered data transfers at 320 Mbytes/sec and was accomplished with the same backplane and cabling used with the existing Ultra160 SCSI standard. Seagate tested numerous industry-leading Ultra160 systems to ensure interoperability between Ultra320 SCSI and Ultra160 SCSI. Ultra320 SCSI technology will enable businesses to move critical data with greater speed and reliability – a must for today's booming Internet economy.

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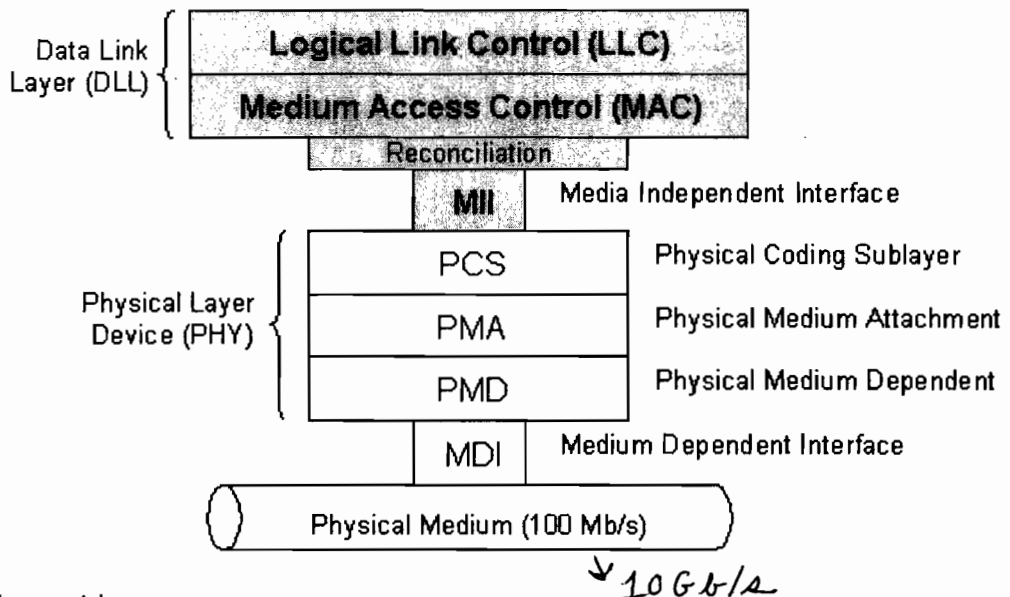
Signal-level transmission variants:

- ***serial copper*** *examples: Glink,(Slink-Glink) CIMT / Gigastar 1.3Gbit. / 8b/10b -Gbit ethernet tranceivers (1.6.. 2.5 Gbps) ,*
- ***parallel copper*** *examples: PECL,, LVDS, Examples serialized LVDS: Channellink, FPD link*
- ***serial optical*** *examples: generated via VCSEL electro-optical converters from serial copper (see CMS Ecal) Agilent fiber optic small formfactor transceivers*
- ***parallel optical*** *examples: Infineon Paroli (12) 1.25/1.5 and 2.5 Gbit/s, (Motorola Optobus), Gore nLighten (12), Mitel MFX 62340 family 12* 2.5 GBps) Common standard agreement on 12 bit wide parallel optical modules (Infineon, Gore, Mitel)*

Serial protocols on top of signal level transmission:

There are two major industry paradigms for encoding: CIMT used in Glink chips (Agilent) is word-synchronous, 8b/10b encoding used in Fiberchannel, Gbit ethernet etc is packet synchronous.

- *Gbit ethernet IEEE802.3 0.1 / 1 Gbit/s copper / fiber* There are 2 interfaces to the MAC layer: a.) IEEE 802.3z Gigabit Media-Independent Interface (GMII) interface for design in point-to-point and backplane applications b.) IEEE 802.3u Standard Media Independent Interface (MII)



Gigabit

Ethernet layers

- Gigabit Ethernet link lengths up to 50 meters will use a single bundle of 4-pair copper UTP-5 wiring
- *IEEE802.3ae task force 10 Gbit/s copper/fiber (codename : XAUI Attachment Unit Interface) the 10 Gigabit ethernet alliance*
- *ATM 0.6 Gbit/s copper*
- *Fiberchannel*
- *Sonet (Synchronous Optical Networks) OC-48 (2.5 Gigabit per second) and OC-192 (10 Gigabits per second)*

PRINTER PORT

IEEE 1284 Electrical Interface

The original parallel port did not have a defined electrical specification that identified the driver, receiver, termination and capacitance requirements in order to guarantee any compatibility between devices. Host adapters and peripherals were built with any number of pull-up values on the control lines, open collector or totem pole drivers for the data and control lines, and most offensive of all, up to 10,000pF capacitors on the data and strobe lines. This type of design variation makes it impossible to create a new interface protocol without explicitly defining the required electrical parameters with which to guarantee operation.

The 1284 standard defines two levels of interface compatibility, Level I and Level II. The Level I interface is defined for products that are not going to operate at the high speed advanced modes, but need to take advantage of the reverse channel capabilities of the standard. The Level II interface is for devices that will operate in the advanced modes, with long cables, and at the higher data rates. This discussion will deal primarily with Level II interfaces. Please refer to the standard for the full requirements for either a Level I or Level II interface.

The requirements for the Level II drivers and receivers are defined at the connector interface. The driver requirements are:

1. The open circuit high-level output voltage shall not exceed +5.5V.
2. The open circuit low-level output voltage shall be no less than -0.5V.
3. The DC steady state, high-level output voltage shall be at least +2.4V at a source current of 14mA.
4. The DC steady state, low-level output voltage shall not exceed +0.4V at a sink current of 14mA.
5. The driver output impedance (Ro), measured at the connector, shall be 50 +/- 5 ohms at 1/2 the actual driver Voh minus Vol voltage.
6. The driver slew rate shall be 0.05-0.40 V/nS

Like the driver requirements, the receiver requirements are defined at the connector interface. The receiver requirements are:

1. The receiver shall withstand peak input voltage transients between -2.0V and +7.0V without damage or improper operation.
2. The receiver high-level input threshold shall not exceed 2.0V
3. The receiver low-level input threshold shall be at least 0.8V.
4. The receiver shall provide at least 0.2V input hysteresis, but not more than 1.2V.
5. The receiver high-level sink current shall not exceed 20uA at +2.0V.
6. The receiver low-level input source current shall not exceed 20uA at +0.8V.
7. Circuit and stray capacitance shall not exceed 50pF.

Figure 1 shows the recommend termination for a driver/receiver pair. Ro represents the output impedance at the connector. It is intended that this impedance match the cable impedance so as to minimize the noise caused by mismatched impedances. Depending upon the type of driver used, a series resistor, Rs may be required to obtain the correct impedance.

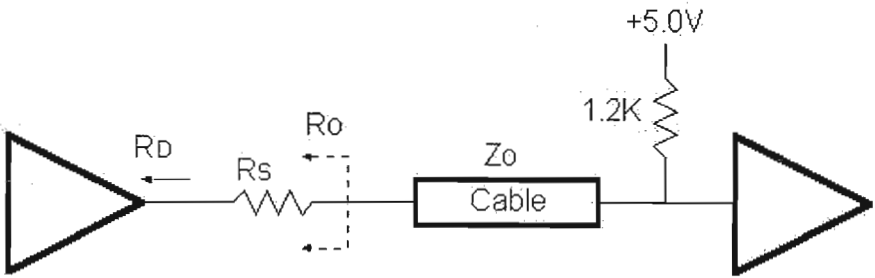


Figure 1 -- Level II Driver/Receiver Pair Termination Example

Figure 2 shows the recommended termination for a Level II transceiver pair, such as the data lines.

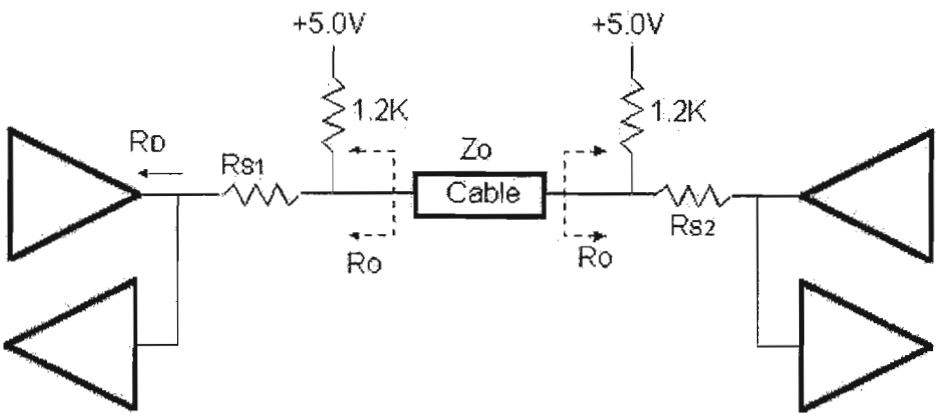


Figure 2 -- Level II Transceiver Termination Example

There are products being introduced by companies such as Texas Instruments and National that provide integrated solutions for a 1284 Level II interface. These include active drivers and receivers as well as resister sip networks.

NOTE: When ECP was first introduced Microsoft made a recommendation for an electrical and termination requirement that was not consistent with the 1284 specification. This included an AC terminator for each of the lines. This suggestion has since been retracted and the current recommendation is to use the interface defined in the IEEE 1284 specification.

Compatibility Mode

This mode defines the protocol used by most PCs to transfer data to a printer. It is commonly called the "Centronics" mode and is the method utilized with the standard parallel port. In this mode, data is placed on the port's data lines, the printer status is checked for no errors and that it is not Busy, and then a data Strobe is generated by the software to clock the data to the printer. Figure 1 describes this transfer.

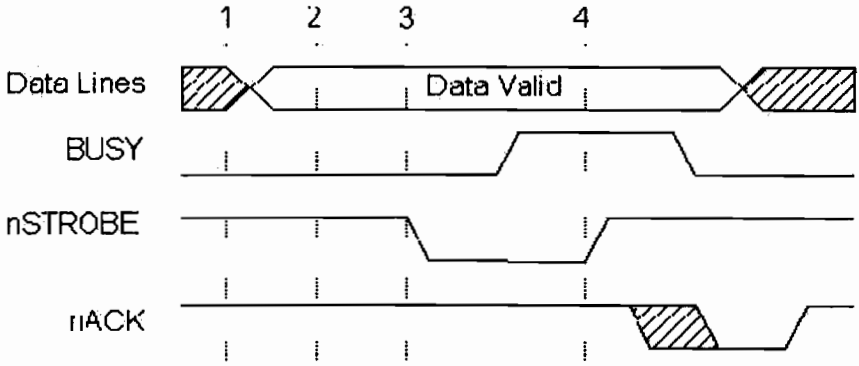


Figure 1 -- Compatibility Mode Data Transfer Cycle

Compatibility Mode phase transitions:

1. Write the data to the data register
2. Program reads the status register to check that the printer is not BUSY
3. If not BUSY, then Write to the Control Register to assert the STROBE line
4. Write to the Control register to de-assert the STROBE line

As can be seen, in order to output one byte of data it requires four I/O instructions and at least as many additional instructions. The net effect of this is a limitation on the bandwidth capabilities of the port on the order of 150K bytes per second. This bandwidth is sufficient for communicating with dot matrix and many older laser printers, but a limitation when communicating with pocket LAN adapters, removable disk drives, and the newest generation of laser printers, to name a few. Of course, this mode is for the forward channel only and must be combined with a reverse channel mode in order to have a complete bi-directional channel. This mode was included as a way to provide backward compatibility with the huge base of installed printers and peripherals. The other modes are used to provide the reverse channel and high performance communication links. Many of the integrated 1284 I/O controllers have implemented a mode that uses a FIFO buffer to transfer data with the Compatibility mode protocol. This mode is referred to as "Fast Centronics" or "Parallel Port FIFO Mode". When this mode is enabled, data written to the FIFO port will be transferred to the printer using hardware generated strobes for the handshaking. Since there is very little latency between transfers, and the software does not have to do any of the strobing or handshake checking, data rates over 500K bytes per second are achievable with some systems. This mode, however, is not an IEEE 1284 defined mode and is not described in the standard.