# CMSC421. Spring 2003. All sections.
Homework I
You must do this HW on your own

1. Five jobs are waiting to be run. Their expected run times are 9, 6, 3, 5 and X. In what order should they be run in order to minimize average waiting time? (Hint: Though the answer is simple, you need to consider all cases).

2. This problem deals with real time systems with N CPU's. Events that real time systems have to respond to are classified as **periodic** or **aperiodic**. Consider the first case where jobs occur at regular intervals: Let there be m periodic events and event i occurs with period P_i and C_i seconds of CPU time are required to handle each event, derive an inequality that can be used to show the conditions under which the periodic load can be handled. (**Hint**: Define CPU utilization, ignore context switch overhead.)

3. For the bakery algorithm we define a processor is in the **bakery** from when it sets **choosing[i] = false** till it fails or leaves the **critical section.** The two lines before it is in the CS it called as being in the **doorway**. Prove the following assertions:

   a. **Assertion 1**: If processors i, k are in the bakery and i entered the bakery before k entered the doorway, then number[i] < number[k].
   b. **Assertion 2**: If processor i is in its critical section, processor k is in the bakery, and k .not equal. i, then (number[i] , i) < (number[k] , k).

4. A computer has six tape drives, with n processes competing for them. Each process may need two drives. For which values of n is this system safe?

5. Consider a system consisting of m resources of the same type, being shared by n processes. Resources can be requested and released by processes only one at a time. Show that the system is deadlock free if the following two conditions hold:
   a. The max need of each process is between 1 and m resources
   b. The sum of all max needs is less than m + n

6. If an instruction takes 1 microsec and a page fault takes an extra n microsec, derive a formula for the effective instruction time if page faults occur every k instructions (on average).

7. The figure below shows a virtual address space from 0 to 64K and 32K of physical memory. There are 16 pages and 8 frames and transfers between memory and disk are in pages. Give the physical address corresponding to the following virtual addresses: a) 20 b) 4100 c) 8300
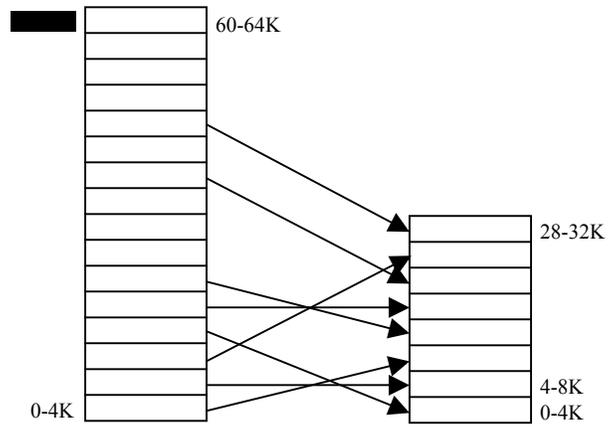
8. Solve problem 10.10 in our textbook.

9. Solve problem 10.11 in our textbook.