CMSC 411 - Section 101 **TEST #2** **7 December 1994**
Computer Architecture

Please return your copy of the test along with your answers.

As an incentive for admitting you have no idea how to answer a question, you'll get 20% credit if you say you don't know the answer (or leave it blank). You can still get partial credit, of course, so please do answer questions you think you know even if you don't know the whole answer.

Please show all your work – I can't give you partial credit for a wrong answer unless I see how you arrived at the answer. Remember, "the journey is as important as the destination."

Good luck!

1. [15] How many tag bits must be maintained for a 2-way set-associative cache with 32 byte blocks that holds 64 KB of data? Assume addresses are 32 bits long. First, calculate the number of tag bits associated with entry, and then use that information to figure out how many tag bits the entire cache must store.

   Give two additional status bits that the cache might have to store for cache entries, and briefly explain their uses.

2. [10] What is a TLB? Give one advantage and one disadvantage of a fully associative TLB, and one advantage and one disadvantage to using a set-associative TLB.

3. [10] You're a designer considering two different memory system designs that use both cache memory and DRAM. The first design uses a 32 KB direct-mapped cache with 32 byte blocks, giving a hit rate of 90% with an access time of 10 ns. The DRAM for this design has an access time of 80 ns. The second design uses a 64 KB 2-way set-associative cache with 64 byte blocks, giving a hit rate of 95% with an access time of 12 ns. The DRAM for the second design has an access time of 100 ns. Which design has a shorter average access time? How will the overall bandwidth of the faster system be affected if cycle time for the DRAM is twice access time? Explain briefly.

4. [10] Give two advantages and one disadvantage for using separate instruction and data caches. Do the same for a unified cache.

5. [10] Explain *briefly* (one sentence) and give one advantage and one disadvantage for each of the following methods for I/O: programmed I/O, DMA, and channel-based I/O.

6. [10] What are the benefits from multiplexing data and address on a single set of wires in a bus? What are the drawbacks? Under what types of use do multiplexed data/address buses perform best?

7. [15] Draw and label the arbitration signals (bus grants, bus requests, bus busy) and devices for a bus with a single arbiter and four devices. The bus supports three bus request/bus grant levels, with 0 the lowest priority and 2 the highest. The bus grant lines are daisy chained through each device.

   While the bus is idle (not busy), all of the devices simultaneously request the bus. Device 4 (counting from the bus arbiter) uses level 0, device 1 uses level 1, and devices 2 and 3 use request level 2. Show the resulting signal levels (0 or 1) on each signal segment (bus requests, grants, and bus busy) just before the bus busy line is asserted. Which device will assert the bus busy line?

8. [10] Draw a asynchronous bus transaction that transfers a word from the bus master to the bus slave with two-way handshaking. Assume the master already has control of the bus. Your diagram should include VALID, ACK, and a single line representing the data lines. Label each edge with a number indicating the order in which the edges occur.

9. [10] A particular synchronous bus requires three cycles for arbitration and one cycle to send the address for a block transfer. It is capable of transferring a full 32-bit word of data each cycle thereafter until the end of the block transfer. If the bus cycle time is 100 ns, what is the peak bandwidth of the bus (assuming an infinitely long transfer)? What is the bandwidth if block transfers are limited to 64 bytes?