Combinational logic accepts inputs and produces output after some delay.

Truth table = circuit diagram = VHDL code

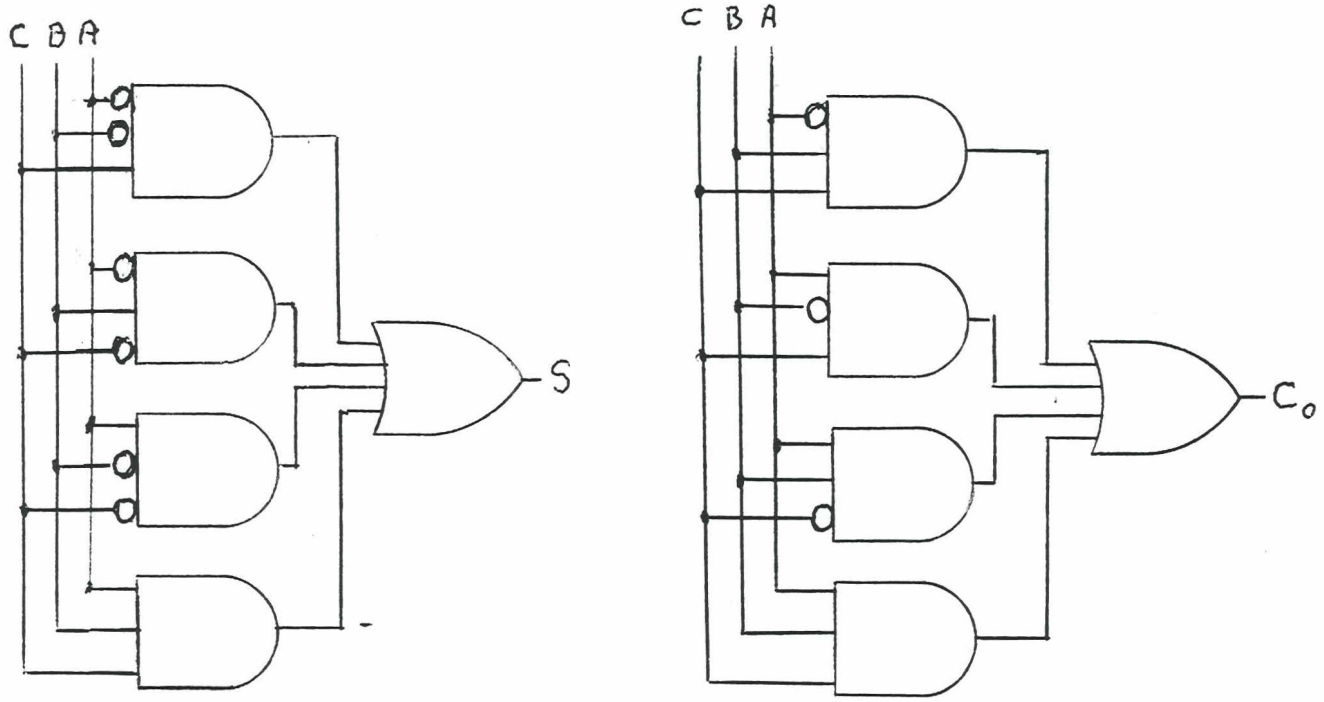
inputs		outputs	
A	B	C	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

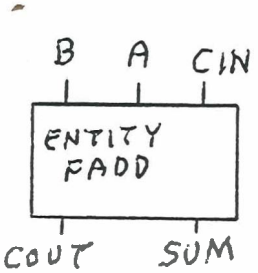
unoptimized VHDL from truth table

```
S <= (not A  and  not B  and      C) or
     (not A  and      B  and  not C) or
     (    A  and  not B  and  not C) or
     (    A  and      B  and      C) after 1 ns;

Co <= (not A  and      B  and      C) or
      (    A  and  not B  and      C) or
      (    A  and      B  and  not C) or
      (    A  and      B  and      C) after 1 ns;
```

unoptimized circuit diagram from truth table





Sequential circuits have storage elements (registers of flip flops)

Combinational circuits MUST NOT HAVE LOOPS !

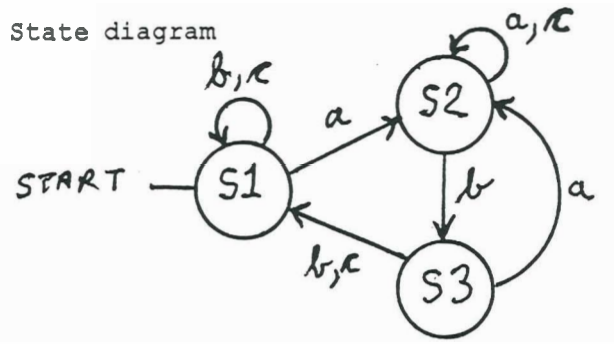
Any feedback loop must have a clocked storage element otherwise is may become locked in one state or may become an oscillator.

State transition table = State diagram = Circuit diagram = VHDL code

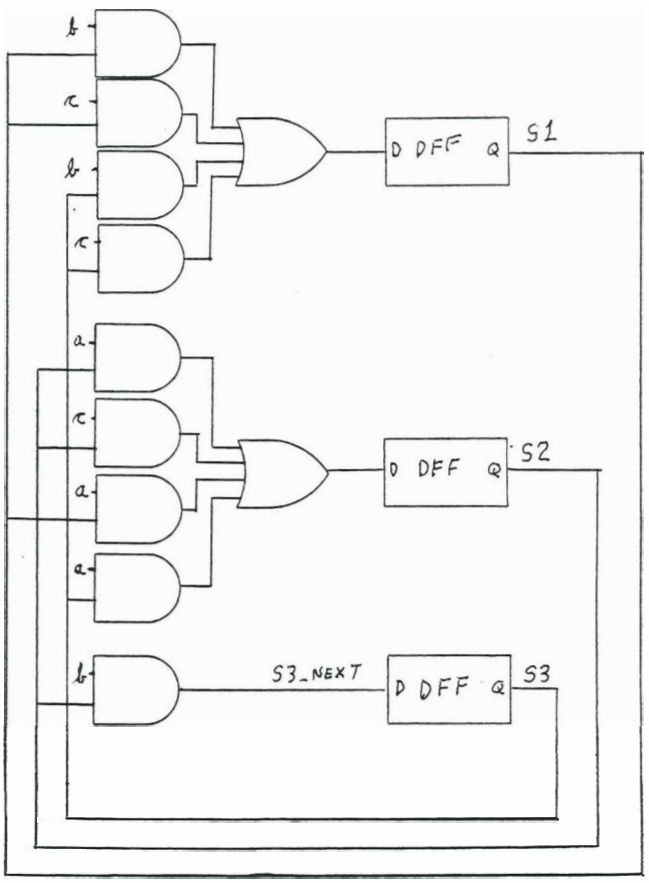
State transition table

state	inputs		
	a	b	c
S1	S2	S1	S1
S2	S2	S3	S2
S3	S2	S1	S1

State diagram



Circuit diagram (unoptimized)



unoptimized VHDL code

```
S1_next <= (S1 and b) or (S1 and c) or (S3 and b) or (S3 and c) after 1 ns;
S2_next <= (S2 and a) or (S2 and c) or (S1 and a) or (S3 and a) after 1 ns;
S3_next <= (S2 and b) after 1 ns;
S1_dff: entity work.dff port map(S1_next, clk, '1', start, S1);
S2_dff: entity work.dff port map(S2_next, clk, start, '1', S2);
S3_dff: entity work.dff port map(S3_next, clk, start, '1', S3);
```